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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
VUONG, QUOCHIEN B	
ART UNIT	**PAPER NUMBER**
2685	

DATE MAILED: 06/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/707,447	SUGAR ET AL.	
	Examiner	Art Unit	
	Quochien B Vuong	2685	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,13-24,32 and 34-38* is/are rejected.

7)☒ Claim(s) *10-12,25-31 and 33* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 3/19/04, 3/22/04, & 1/10/05.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statements (IDSs) submitted on 03/19/2004, 03/22/2004, and 01/10/2005 are in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statements are being considered by the examiner.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-9, 13-24, 32, and 34-38 are rejected under 35 U.S.C. 102(b) as being anticipated by Lipperer et al. (GB 2349309 A).

Regarding claim 1, Lipperer et al. (figure 2) disclose a method for connecting signals between a radio integrated circuit (IC) (1) and a signal processing device (36) comprising the step of multiplexing two or more signals on a connection pin (28-31 and 40-43) between the radio IC and the signal processing device (page 6, line 34 - page 10, line 11).

Regarding claim 2, Lipperer et al. disclose the step of multiplexing comprises multiplexing transmit and receive signals on the connection pin such that during a transmit mode a transmit signal is coupled on the connection pin from the signal

processing device to the radio IC, and during a receive mode a receive signal is coupled from the radio IC on the connection pin to the signal processing device (page 7, line 25 - page 10, line 11).

Regarding claims 3-5, Lipperer et al. disclose the multiplexing step is performed on each of a plurality of cennection pins between the radio IC and the signal processing device for a plurality of corresponding transmit and receive signals, a connection pin for transmit and receive in-phase (I) signals and transmit and receive quadrature (Q) signals, or each of a pair of connection pins associated with differential transmit signals and differential receive signals (page 7, line 25 - page 10, line 11).

Regarding claim 6, Lipperer et al. disclose in a transmit mode, the step of multiplexing comprises multiplexing a transmit in-phase (I) signal and transmit quadrature (Q) signal on a connection pin between the radio IC and the signal processing device (page 7, line 25 - page 10, line 11).

Regarding claim 7, Lipperer et al. disclose in a receive mode, the step of multiplexing comprises multiplexing a receive in-phase (I) signal and receive quadrature (Q) signal on a connection pin between the radio IC and the signal processing device (page 7, line 25 - page 10, line 11).

Regarding claim 8, Lipperer et al. (figure 2) disclose a radio transceiver IC (1) comprising: at least one receiver (page 7, lines 1-3) that produces a receive signal and at least one transmitter (page 7, lines 3-6) that processes a transmit signal for transmission; and a connection pin that couples the transmit signal supplied to the radio IC for processing by the transmitter during a transmit mode and couples as output the

receive signal produced by the receiver during a receive mode (page 6, line 34 - page 9, line 20).

Regarding claim 9, Lipperer et al. disclose a switch coupled to the connection pin that in a first position during the transmit mode couples the connection pin to the transmitter to connect the transmit signal to the radio IC, and in a second position during the receive mode couples the connection pin to output the receive signal produced by the receiver (page 7, line 25 - page 10, line 11; and figure 2).

Regarding claim 13, Lipperer et al. disclose wherein the at least one transmitter and at least one receiver each have an in-phase (I) signal path and a quadrature (Q) signal path, and further comprising a connection pin associated with the in-phase (I) signal path that is shared for a transmit I signal or a receive I signal, and a connection pin associated with the quadrature (Q) signal path that is shared for a transmit Q signal or a receive Q signal (page 7, line 25 - page 10, line 11; and figure 2).

Regarding claim 14, Lipperer et al. disclose further an analog-to-digital converter (ADC) (37) that is coupled to the connection pin that in the receive mode converts the receive signal to a digital signal and a digital-to-analog converter (DAC) (38) that in the transmit mode converts the transmit signal to an analog signal that is coupled to the connection pin, and a control circuit that controls the ADC and the DAC such that in the receive mode, the DAC is switched to a power down mode which has a high impedance at the DAC output to minimize signal coupling from the output of the DAC onto the connection pin, and during the transmit mode, a sample clock of the ADC is held in a hold state to create a high input impedance at the ADC input to minimize

signal coupling from the DAC into the input of the ADC (page 7, line 25 - page 10, line 11).

Regarding claim 15, Lipperer et al. (figure 2) disclose a signal processing device (36) coupled to the radio IC via the connection pin, and wherein the ADC, DAC and control circuit are part of the signal processing device and the signal processing device produces the transmit signal and processes the receive signal output by the radio IC (page 7, line 25 - page 10, line 11).

Regarding claim 16, Lipperer et al. (figure 2) disclose a signal processing device (36) coupled to the radio IC via the connection pin, wherein the signal processing device produces the transmit signal and processes the receive signal output by the radio IC (page 7, line 25 - page 10, line 11).

Regarding claim 17, Lipperer et al. disclose wherein the transmitter and receiver each have differential signal paths, and further comprising a pair of connection pins that are shared to couple differential transmit signals supplied to the radio IC for processing by the transmitter during the transmit mode and to couple as output differential receive signals produced by the receiver during the receive mode (page 7, line 25 - page 10, line 11; and figure 2).

Regarding claim 18, Lippere et al. (figure 2) disclose a radio transceiver integrated circuit (IC) (1) comprising: at least one transmitter (page 7, lines 3-6) and at least one receiver (page 7, lines 1-3), each of which includes an in-phase (I) signal path and a quadrature (Q) signal path; a transmitter connection pin on which a transmit I signal and a transmit Q signal are multiplexed for connection to the respective I and Q

signal paths of the transmitter, and a receiver connection pin on which a receive I signal and a receive Q signal are multiplexed from the respective I and Q signal paths of the receiver (page 6, line 34 - page 9, line 20).

Regarding claim 19, Lippere et al. (figure 2) disclose a first multiplexer circuit that couples from the transmitter connection pin the transmit I and transmit Q signals during different time intervals for connection to the I and Q signal paths, respectively, of the transmitter (page 8, line 29 – page 10, line 3).

Regarding claim 20, Lipperer et al. disclose wherein the first multiplexer circuit alternately couples the transmit I and transmit Q signals, respectively, from the transmitter pin to the I and Q signal paths, respectively, of the transmitter (page 8, line 29 – page 10, line 3).

Regarding claim 21, Lipperer et al. disclose a second multiplexer circuit that couples during different time intervals the receive I and receive Q signals to the receiver connection pin from the I and Q signal paths, respectively, of the receiver (page 7, line 25 – page 8, line 27; and page 10, lines 3-28).

Regarding claim 22, Lipperer et al. disclose wherein the second multiplexer circuit alternately couples the receive I and receive Q signals to the receiver connection pin from the I and Q paths, respectively, of the receiver (page 10, lines 3-28).

Regarding claim 23, Lipperer et al. disclose a multiplexer circuit that during a receive mode couples to the receiver connection pin the receive I and receive Q signals during different time intervals from the I and Q signal paths, respectively, of the receiver, and during a transmit mode, couples from the transmitter connection pin the transmit I

and transmit Q signals during different time intervals to the I and Q signal paths, respectively of the transmitter (page 7, line 25 – page 10, line 28).

Regarding claim 24, Lipperer et al. disclose a timing circuit that supplies a timing signal to the multiplexer circuit to control the timing of the first and second multiplexer circuits (page 7, line 25 – page 10, line 28).

Regarding claim 32, Lipperer et al. disclose wherein each of the I and Q signal paths of the transmitter and receiver are differential, and further comprising a pair of transmitter connection pins on which differential transmit I and transmit Q signals are multiplexed, and a pair of receiver connection pins on which differential receive I and receive Q signals are multiplexed (page 7, line 25 – page 10, line 28).

Regarding claim 34, Lipperer et al. (figure 2) disclose a signal processing device (36) coupled to the radio IC that supplies the transmit I signal and transmit Q signal to the radio IC for transmission processing and processes the receive I signal and receive Q signal from the radio IC (page 7, line 25 - page 10, line 11).

Regarding claim 35, Lipperer et al. (figure 2) disclose a timing circuit in the radio IC and a timing circuit in the signal processing device, wherein the timing circuit in the radio transceiver or timing circuit in the signal processing device generates timing signals that are coupled to the other timing circuit in order to coordinate the transfer of transmit I and transmit Q signals from the signal processing device to the radio IC and to coordinate transfer of the receive I and receive Q signals from the radio IC to the signal processing device (page 7, line 25 - page 10, line 11).

Regarding claim 36, Lipperer et al. (figure 2) disclose wherein the radio IC further

comprises at least one multiplexer circuit coupled to the timing circuit in the radio IC and is responsive to timing signals supplied by the timing circuit to couple from the transmitter connection pin the transmit I and transmit Q signals during different time intervals for connection to the I and Q signal paths, respectively, of the transmitter, and to couple to the receiver connection pin the receive I and receive Q signals during different time intervals from the I and Q signal paths, respectively, of the receiver (page 7, line 25 - page 10, line 11).

Regarding claim 37, Lipperer et al. (figure 2) disclose a method for connecting signals between at least one of a radio transmitter (page 7, lines 3-6) and a radio receiver (page 7, lines 1-3) and a signal processing device (36), the method comprising the step of multiplexing two or more signals on a connection pin between the signal processing device and one or both of the radio transmitter and radio receiver (page 6, line 34 - page 9, line 20).

Regarding claim 38, Lipperer et al. disclose the step of multiplexing comprises multiplexing transmit and receiver signals on the connection pin such that during a transmit mode a transmit signal is coupled on the connection pin from the signal processing device to the radio transmitter, and during a receive mode a receive signal is coupled from the radio receiver on the connection pin to the signal processing device (page 6, line 34 - page 9, line 20).

Allowable Subject Matter

4. Claims 10-12, 25-31, and 33 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Regarding claim 10, Lipperer et al. disclose the radio IC of claim 8 above. However, Lipperer et al. fail to teach or fairly suggest further a plurality of transmitters and a plurality of receivers such that pair of a transmitter and a receiver are associated with a corresponding one of a plurality of antennas connected to the radio IC, and further comprising a plurality of connection pins each associated with a corresponding transmitter/receiver pair that couples a corresponding transmit signal to the radio IC during the transmit mode for transmission processing and couples a corresponding receive signal produced by a corresponding receiver during the receive mode.

Regarding claims 25 and 33, Lipperer et al. disclose the radio transceiver IC of claim 18 and 32, respectively above. However, Lipperer et al. fail to teach or fairly suggest further a plurality of transmitters and a plurality of receivers such that a pair of a transmitter and a receiver are associated with a corresponding one of a plurality of antennas connected to the radio IC, and further comprising a plurality of transmitter connection pins each associated with a corresponding transmitter and a plurality of receiver connection pins each associated with a corresponding receiver, each transmitter connection pin on which corresponding transmit I and transmit Q signals are multiplexed for connection to the I and Q signal paths, respectively, of the associated transmitter and each receiver connection pin on which corresponding

receive I and receive Q signals are multiplexed for connection from the I and Q signal paths, respectively, of the associated receiver.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quochien B Vuong whose telephone number is (571) 272-7902. The examiner can normally be reached on M-F 9:30-18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward Urban can be reached on (571) 272-7899. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

QUOCHIEN B. VUONG
PRIMARY EXAMINER

Quochien B. Vuong
June 01, 2005.